This Standard received approval from the NMRA membership and Board of Trustees in January 1994 and July 2002. An additional revision (in red) was approved by the BOT in July 2003 for the next membership vote.

Communication from a Digital Command Station to a Digital Decoder is accomplished by transmitting a series of bits that convey instructions. A bit is a signal which represents one of two conditions, which we will call "1" and "0". This portion of the standard covers the electrical characteristics of the digital command control signal that encodes these bits.

A: Technique For Encoding Bits

The NMRA baseline digital command control signal consists of a stream of transitions between two equal voltage levels that have opposite polarity[1]. Alternate transitions separate one bit from the next. The remaining transitions divide each bit into a first part and a last part. Digital Command Stations shall encode bits within this digital command control stream of transitions by varying the duration of the parts of the bits, or frequency of the transitions.

In a "1" bit, the first and last part of a bit shall have the same duration, and that duration shall nominally be 58 microseconds[2], giving the bit a total duration of 116 microseconds. Digital Command Station components shall transmit "1" bits with the first and last parts each having a duration of between 55 and 61 microseconds. A Digital Decoder must accept bits whose first and last parts have a duration of between 52 and 64 microseconds, as a valid bit with the value of "1".

In a "0" bit, the duration of the first and last parts of each transition shall nominally be greater than or equal to 100 microseconds. To keep the DC component of the total signal at zero as with the "1" bits, the first and last part of the "0" bit are normally equal to one another. Digital Command Station components shall transmit "0" bits with each part of the bit having a duration of between 95 and 9900 microseconds with the total bit duration of the "0" bit not exceeding 12000 microseconds. A Digital Decoder must accept bits whose first or last parts have a duration of between 90 and 10000 microseconds as a valid bit with the value of "0". Figure 1 provides an example of bits encoded using this technique.

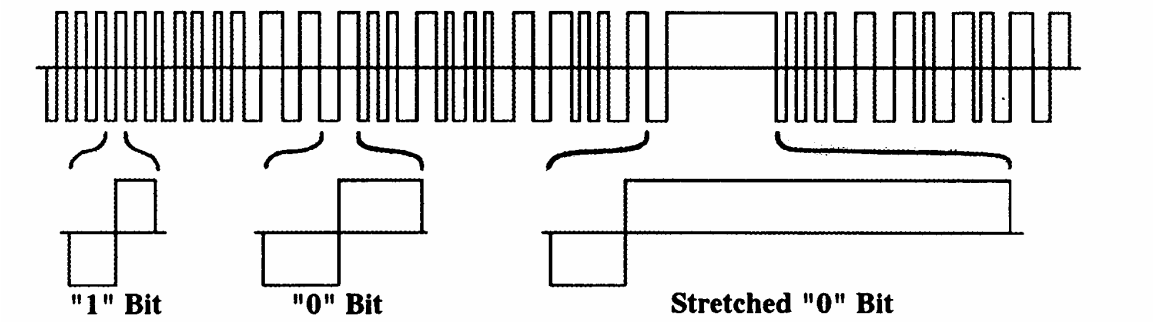


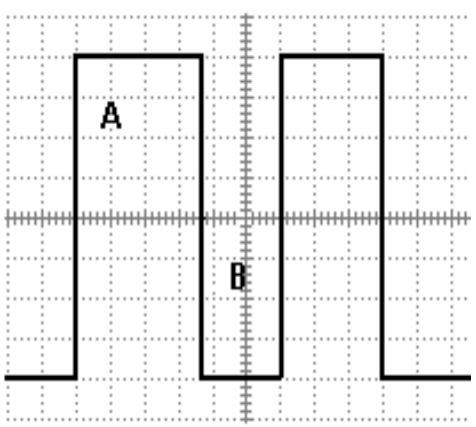
Figure 1: Bit Encoding

Digital Decoders must accept one bits whose positive and negative components differ by as much as 6 microseconds.

[1] Note that since a locomotive or piece of rolling stock can be placed upon a given section of track facing in either direction, it is impossible to define, from the point of view of a *Digital Decoder*, whether the first or last part of a bit will have the "positive" voltage polarity.

[2] All timing measurements are done between zero volt crossings.

One Bit Timing



For **Power Station** Output under Load:

Relationship for One Bits	Result
Period A < 55 µSec or Period A > 61 µSec	Bad
Period A = Period B	OK
|Period A – Period B| <= 3 µSec	OK
|Period A – Period B| > 3 µSec	Bad

Decoders must accept:

Relationship for One Bits	Result
Period A >= 52µSec and Period A <= 64 µSec	OK
Period A = Period B	OK
|Period A – Period B| <= 6 µSec	OK

B: Command Control Signal Shape

The NMRA digital signal applied to the track by any Digital Command Control system, as measured at the power station output, shall have the following characteristics, as measured under conditions ranging from no load to the maximum continuous load permitted by the power source. Transitions that cross the region between -4 volts and +4 volts[3] shall occur at 2.5 volts per microsecond or faster. This signal may contain non-monotonic distortion at the zero-crossing transitions, provided that this distortion shall have an amplitude of no greater than +/- 2 volts[4].

Digital Decoders shall be designed to correctly decode signals with transitions whose slope is 2.0 volts per microsecond or faster across the voltage range from -4 volts to +4 volts. A Digital Decoder shall correctly decode at least 95% of properly addressed baseline packets, as defined in S-9.2, in the presence of noise (and/or other types of signals) above 100 kHz with a total peak-to-peak amplitude of less than one fourth of the peak-to-peak amplitude of the NMRA digital signal[5].

The exact shape of the NMRA digital signal shall be designed to minimize electromagnetic radiation such that a large layout operated using this standard can meet applicable United States Federal Communications Commission electromagnetic interference requirements[6].

[3] 0 volts is the mid point of the differential voltage.

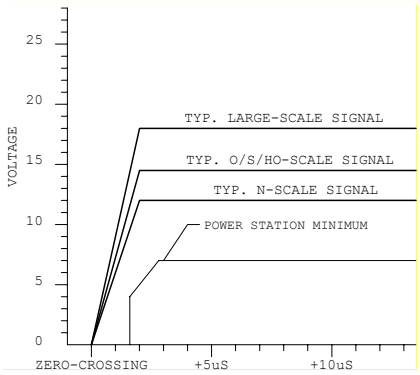
[4] This standard specifically permits super-imposing non-NMRA signals upon the rails for other purposes, provided that the NMRA Digital Decoder can reject these signals.

[5] This measurement is made with the Digital Decoder electrically connected to a track or accessory bus.

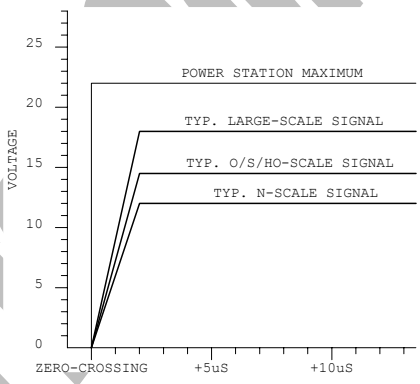
[6] All components of a NMRA compliant digital system shall meet all applicable FCC and/or CE requirements.

C: Power Transmission and Voltage Limits For Transmitting Power Through the Rails

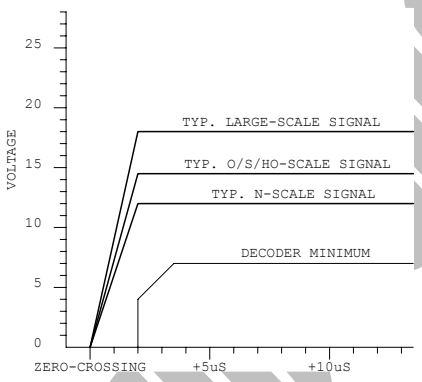
The baseline method for providing the power to operate locomotives and accessories, which shall be supported by all Digital Command Stations and Digital Decoders, is by full-wave rectification of the bipolar NMRA digital signal within the Digital Decoder[7]. In order to maintain power to the Digital Decoders, gaps in bit transmission are only allowed at specified times (see S-9.2, Section C). The RMS value of NMRA digital signal, measured at the track, shall not exceed by more than 2 volts[8] the voltage specified in standard S9 for the applicable scale[9]. In no case should the peak amplitude of the command control signal exceed +/- 22 volts. The minimum peak value of the NMRA digital signal needed to provide power to the decoder shall be +/-7 volts measured at the track. Digital Decoders intended for "N" and smaller scales shall be designed to withstand a DC voltage of at least 24 volts as measured at the track. Digital Decoders intended for scales larger than "N" shall be designed to withstand a DC voltage of at least 27 volts as measured at the track.



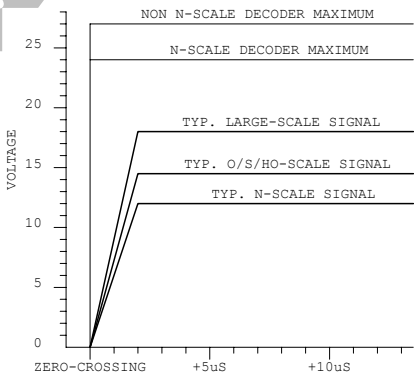
Minimum Voltage for Power Stations



Maximum Voltage for Power Stations



Minimum Voltage for Decoders



Maximum Voltage for Decoders

[7] Alternate means for supplying power are acceptable, provided that *Digital Command Station* power units are capable of producing the baseline track signal, and Digital Decoders are capable of operation from the baseline track signal as described by this standard.

[8] The additional voltage is to compensate for voltage drop in the *Digital Decoder*, to ensure that the maximum voltage as specified in the NMRA Electrical Standard (S-9) is available at the motor brushes.

[9] Care should be taken to ensure that any motors exposed directly to the digital signal for extended periods have a stall rating that exceeds the amplitude of the signal, or sufficiently high impedance at 4-9 kHz to reduce the current to normal operating level. This appears to only be a concern for high-precision core-less can motors, which present a low impedance load, or for layouts using an NMRA digital signal with an amplitude in excess of +-18 volts.